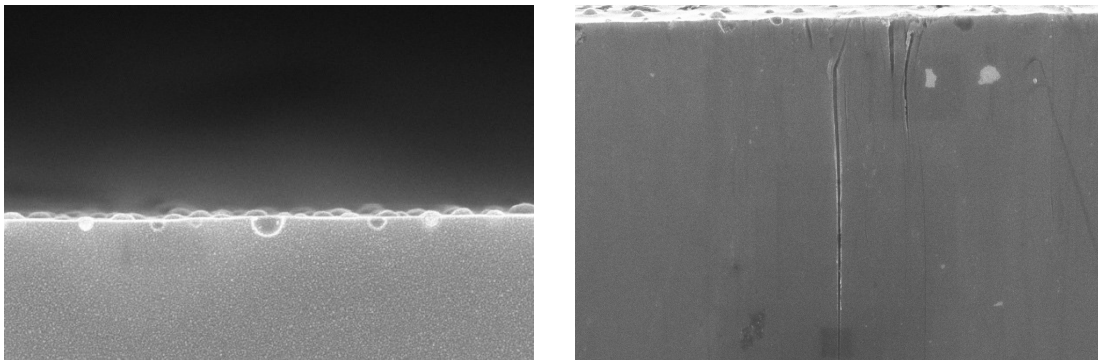


ETCHING OF QUARTZ WITH THE AID OF GOLD NANOPARTICLES

MD. SAJED RABBANI



MSc Thesis
December 2018
Department of Physics and Mathematics
University of Eastern Finland

Md. Sajed Rabbani

Etching of quartz with the aid of gold nanoparticles, 6 pages

University of Eastern Finland

Master's Degree Programme in Photonics

Supervisors:

Prof. Markku Kuitinen

Ph.D. Petri Karvinen

Abstract

The etching possibility of SiO₂ is studied systematically using gold nanoparticles. Penetration depth, surface diffusion and morphological change of gold nanoparticles deposited in a silica substrate have been investigated. Results of different process parameters such as deposition rate and annealing effect etc. were also investigated against different substrates and patterning methods. Gold nanoparticles were formed by annealing a thin sputter coated gold film. Lift off process followed by standard photolithography and shadow mask processes were used to pattern the gold film in the silicon substrate before annealing. Furthermore, bulk gradient process is used to compare the difference on result parameters between patterned and unpatterned substrate.

The thickness of gold used in this study was 20 nm or 40 nm. The thermal dewetting of the gold nanoparticles deposited in the substrate was carried out by high temperature which was close to 1053°C. Diffusion of gold nanoparticles was found with a diameter range of 35 nm to 225 nm and length up to a range of 30 nm to 200 nm in a 500 µm thick substrate. The parameters were observed through a scanning electron microscope.

Keywords: Gold Nanoparticle, Silica, Nanopore, Annealing, Solid State Dewetting, Nano Fabrication.

Preface

This thesis is the final work of my master's studies in University of Eastern Finland. Firstly, I would like to express my deepest gratefulness and honor to my supervisors Prof. Markku Kuittinen and Ph.D. Petri Karvinen for all the guiding's to successfully carrying out my Master's thesis and offering all the possible conveniences for this study. I have gained a lot of practical and theoretical information's related to the micro- and nanofabrication throughout the whole work by being a fellow of such amazing, well informed and experienced supervisors. I am more than grateful to them for patiently answering all my questions and allowing me to work independently.

I would like to thank present head of the Department of Physics and Mathematics, Prof. Dr. Seppo Honkanen for helping me throughout the study. I am truly thankful to Prof. Dr. Kai-Erik Peiponen for guiding me throughout the studies successfully. I am grateful to Dr. Matthieu Rousey for giving me the first opportunity to work in the world class clean-room facility of this university. I thank all professors, researchers and staffs of this wonderful department from whom I have learnt a lot of. I am ever grateful to Noora Heikkila for providing and guiding me to the best possible administrative and academic support. I am thankful to all of my classmates for their wonderful support and encouragement during the studies. I am also grateful to my friend Khairul Alam, former graduate and PhD student of the department, for his superior guidance and support.

I cannot express in words about the endless gratitude towards my parents, Dr. Rabbani and Samina for all their sacrifices in achieving my goals in every sphere of life to provide me all the possible academic, mental and family support.

Finally, I am extremely happy to express my gratitude to almighty Allah for blessing me to complete my thesis successfully.

Joensuu, the 14th of March 2019

Md. Sajed Rabbani

1 Introduction	1
2 Theory	3
2.1 Patterning	4
2.1.1 Photolithography	4
2.1.2 Electron Beam Lithography.....	6
2.1.3 Resist	7
2.1.4 Shadow mask.....	8
2.2 Thin Film Deposition.....	9
2.3 Pattern Transferring by Lift off.....	11
2.4 Thermal Dewetting.....	13
3 Etching Proedure by Gold Nanoparticles	14
3.1 Sample Processing.....	14
3.1.1 Wafer cleaning.....	14
3.1.2 Oxide growth.....	15
3.2 Patterning by Photolithography process.....	15
3.2.1 Resist spinning & Soft bake.....	15
3.2.2 Exposure	16
3.2.3 deposition of gold.....	16
3.2.4 Resist Development.....	17
3.2.5 Lift of.....	17
3.3 Patterning by Shadowmask process.....	17
3.4 Patterning by Bulk gradient process.....	18
3.5 Oven treatment.....	19
3.6 Characterization.....	19
3.6.1 Conductive layer coating.....	20
3.6.2 Scanning Electron Microscope Imaging.....	20
4 Results and Discussions	21
4.1 Effect of using different samples.....	21
4.2 Effect of different deposition rate.....	22
4.3 Effect of annealing.....	23
4.4 Result of lift off	24
4.5 Result of bulk gradient process.....	26
5 Conclusions	29

Bibliography	31
Appendix A	
Used Equipment's	36

CHAPTER 1

Introduction

In Micro and nanofabrication process sphere, etching is referred as the removal of a certain material from the substrate surface. Etching is generally used in fabrication of semiconductor devices for pattern transfer, wafer planarization and isolation. The process is prepared with the assistance of lithography process to select particular areas of the substrate from where the material is removed. Until the late 1970's, wet etching was the preferred technique for transferring pattern in the field of integrated circuit fabrication procedure [1]. The revolutionary invention of plasma based etching substituted wet etching in fabrication process. It is when Stephan Irving successfully demonstrated the process of removing photoresist films with reactive oxygen plasma in 1968 [2]. Since then development of plasma based etching started abruptly and was further developed by Irving's invention of gas plasma vapor based etching process in 1971[3]. This invention influenced researchers to think about the appropriate gases to generate plasma. In 1974 Naokichi Hoskawa demonstrated the etching features of fluorine and chlorine-containing gases instead of argon gas to etch materials like Si, quartz, glass, Al, Mo. The process involved two parallel quartz plate reactors along with photoresist to increasing the etch rate of these materials [4]. This selective technique is particularly called reactive ion etching (RIE), reactive sputter etching (RSE) or ion-assisted plasma etching, which went through further development by Hoskawa in 1975, where he exhibited the etching process of Si and SiO₂ in C_nF_m/O₂ and C_nF_m/H₂ plasmas [5]. Since then this distinct model of plasma based dry etching has become the most popular pattern transfer technique and widely used in semiconductor industry [6]. The further development to improve the etching process and to optimize the parameters is still of great interest to researchers.

Quartz is an essential material in the field of optoelectronics and photonics because of its characteristics such as high temperature stability, chemical resistance, high resistivity to laser operation. These properties also resemble the difficulty of using it in fabrication process. Most common methodology to fabricate structures in quartz or fused silica is by patterning the substrate by electron beam lithography, laser ablation, photolithography [7]. While there were, several processes developed to fabricate structures but low etch rate and selectivity were the primary issues to be solved. Previously, etching of quartz was performed by HF, CF₄, SF₆, CHF₃ and various kind of reactive gases via RIE which provide high etch rate [8]. Later on, further developments were done in order to achieve a pattern size smaller than 100 nm with high etch rate and accuracy on the substrate [9].

Evolution of this research area brought drastic changes on the Si integrated circuit industry as the outcome of this can be visible on the microelectromechanical system(MEMS) devices. Nano sized integrated circuit is considered to be the core of these devices [10]. Until now developing the etching process of quartz with high etch rate and selectivity with different particles is on research phase.

Gold is considered to be one of the widely-used material in the MEMS industries because of its high thermal and electrical conductive property and also for its solid bond structure. Another excellent feature for which gold thin film is popular is, its deposition in the substrate by both physical vapor deposition and electrodeposition [11]. The electro optical properties of gold nanoparticles have been developed and characterized by constant research and usage in numerous applications because of its invigorating interaction with visible light spectrum. The application can be tunable depending on the size of the gold nanoparticles deposited on the thin film [12]. Gold nanoparticles of different morphology are also used to generate and enhance the sensitivity of Surface-enhanced Raman spectroscopy which eventually led into scope of studies for biological and gas sensors. Today high surface to volume aspect ratio of gold nanoparticle arrays are widely used in photodynamic therapy molecular sensing and various kinds of biomedical sensing applications [13,14]. The main objective in this study is to observe and experiment the etching possibility of quartz by gold nanoparticles which is one of the vital component in fabrication industry for the application of DNA sequencing, molecular sensing and molecular separations.

The whole study was done in cleanroom environment. The etching characteristics of quartz was observed by transferring the gold thin film patterns into the substrate by several techniques (e.g. electron beam lithography, photolithography, lift-off, shadow mask) and was proceeded to oven treatment for thermal dewetting. High temperature(1053°C) which is close to the melting temperature of gold was used for the annealing procedure. Achieved samples were then characterized with a scanning electron microscope (SEM). In this study, Chapter 2 reflects on the theoretical approaches which were taken into account in this fabrication process. Chapter 3 includes the experimental procedures and processes followed during the experiment to provide a brief overview of this method. Comprehensive results are discussed in Chapter 4 with the SEM images. Finally, Chapter 5 draws the conclusion of this experimental procedure.

In this chapter, theoretical explanation of the techniques behind this research has been briefly explained. The evolution of nanotechnology created several cost-efficient nanofabrication techniques which has been under development for decades to minimize the feature size by keeping the high scale resolution. There are several techniques of micro-nano fabrication nowadays which are used for different purposes. In this research, standard photolithography along with lift-off, shadow mask and electron beam lithography techniques were used for patterning. The theoretical description of these techniques is discussed in this chapter along with the parameters that are needed for each of the techniques.

2.1 Patterning

Integrated circuit (IC) fabrication involves a lot of physical and chemical processes to be performed on a semiconductor substrate. In this processes patterning is considered to be the backbone of the fabrication process. Lithography is the technique which is used to create desired geometric pattern from a mask on a thin polymer film which is called resist. Depending on the purpose of the optical function, desired profile and functionality, lithography can be classified into optical lithography, electron beam lithography, X-ray lithography. The detailed classification of the lithography processes is shown in fig.1[15]. Each of the techniques has their advantages, limitations, and provides specific feature size range. In this research Photolithography and electron beam lithography technique are used for the desired patterning.

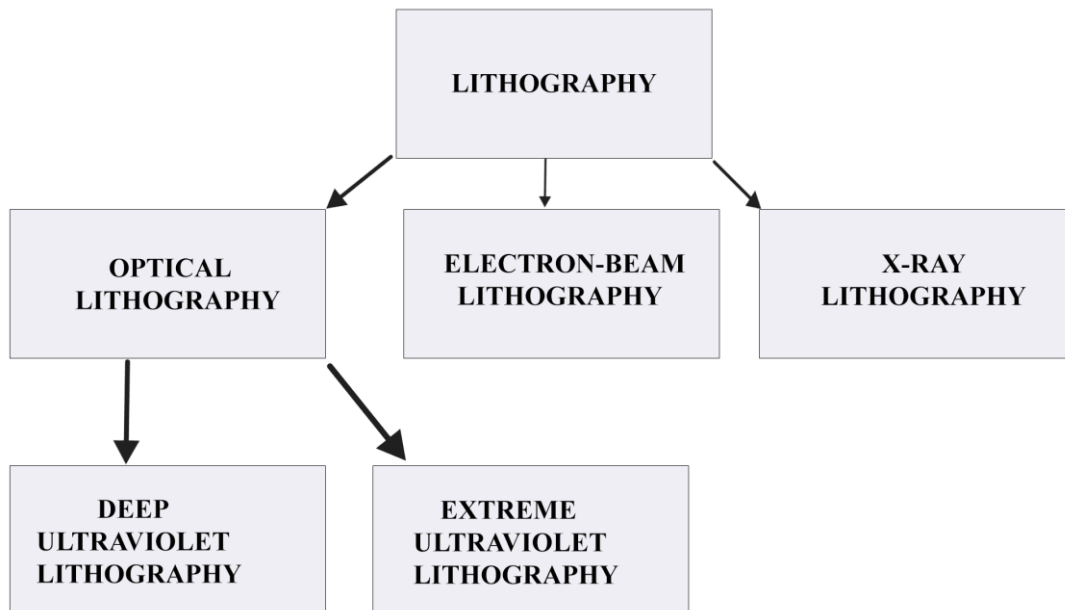


Figure 2.1: Classification of lithography techniques [16].

2.1.1 Photolithography

Photolithography is the most popular and widely used lithographic technique in the patterning process. In this technique, a geometric pattern is transferred to photosensitive film placed on top of the substrate by exposing light with or without an optical mask. Usually ultraviolet radiation is mostly used as the light source. An optical mask is used as a medium which consists of opaque and transparent patterns. When the radiation falls on the mask, light gets passed through the transparent part of the mask and allows the light to fall on the photoresist. Typical optical mask patterns are made of chromium or iron oxide. The resulting pattern on the photoresist is the inverse image of the pattern on the photomask. The pattern on the photoresist is then transferred to the substrate. Different photoresist has different properties which changes when exposed to proper radiation of light. The success of the multilayered structures depends on the alignment of the photomasks and exposure of the successive patterns on the substrate [17]. Figure 2.2 represents the schematic of the photolithography process.

Photolithography systems can be of different types depending on the aligner, which defines the contact of resist with mask. The basic types of aligner are contact, proximity and projection. In the contact printing systems, the resist is directly in contact with the mask providing 1:1 imaging. Whereas, in the proximity system the resist is partially in contact with the mask providing the same magnification by succeeding near field or Fresnel diffraction theory. As they both are in contact and almost in contact with mask they are

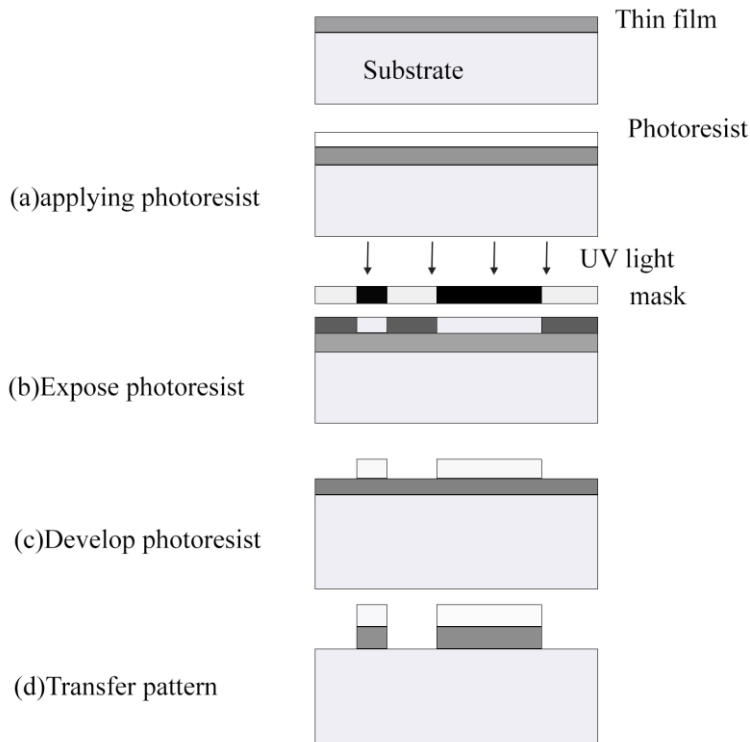


Figure 2.2: Schematic of photolithography process [18].

called diffraction-limited aligners. Whereas, In the projection system, the mask pattern is projected to the photoresist layer with a distance from the mask and demagnified with a magnification, of 1:4-1:10 [19]. This type of aligner is based on far field or Fraunhofer diffraction theory. In Figure 2.3. the demonstration of these 3 aligners is presented.

Issues related to the quality of photolithography systems (e.g. resolution, registration, throughput) has been developed in years [20]. Resolution was one of the parameter that went through major development, which determines the size of the feature. Resolution is defined by the wavelength of incident light (λ) and the numerical aperture (NA) of the lens projecting the image by Rayleigh criteria, $R = \frac{\lambda}{NA}$. Resolution of a system doesn't only depend on the wavelength, numerical aperture and diffraction but it also depends on particular parameters, e.g. depth of focus, thickness of photoresist, and surface roughness. These are the parameters that went through development procedures for decades by scientists [21]. Projection printing which is called 3D-printing nowadays has substituted contact and proximity printings with the aid of developed lens and computer aided software in 1980's. Three main class of projection based printing are: scanning, step-and-repeat, and step-and-scan system [22]. Step-and-scan printing is the technology that has been developed in recent years and it is mainstream choice for lithography instrument manufacturers because of its high resolution, configurability and scalable features. Nowadays, with high aspect ratio step-and-scan printing, it is possible to achieve a resolution of 13nm [23].

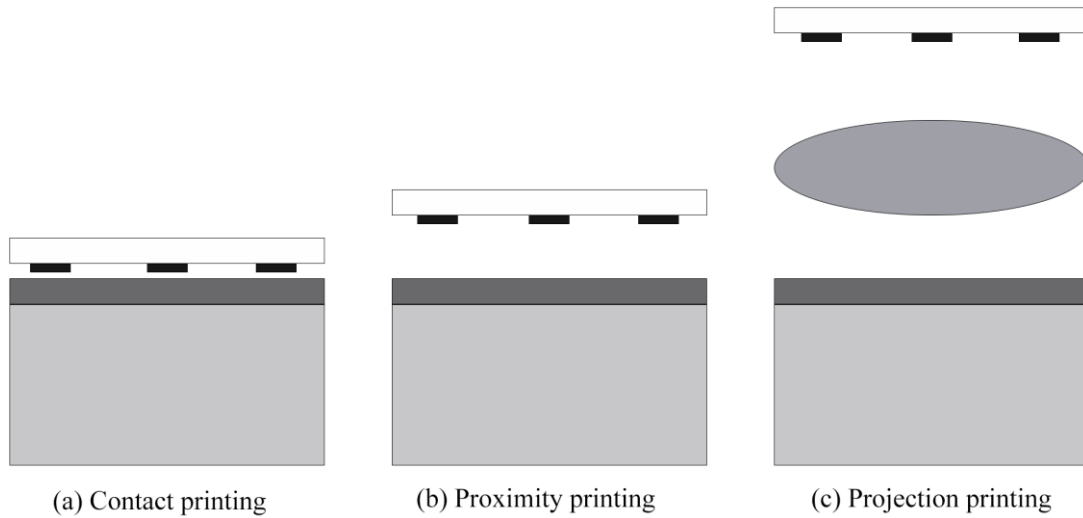


Figure 2.3: Different mask alignment systems. [19]

2.1.2 Electron Beam Lithography

Electron Beam Lithography (EBL) is one of the most popular lithography techniques which is renowned for providing high precision. It was discovered in 1960's to scan tiny substances with electrons and easily modifying the patterns. Conventional lithographic approaches bending of light using mirrors whereas in EBL the process involves bending of electrons using force [24]. The two types of forces used to bend electrons are -electromagnetic and electrostatic, which are used to manufacture electromagnetic and electrostatic lenses to focus electrons. This technique is mask-less and pattern on the substrate is written upon like with a pencil.

A conventional EBL system involves of an electron gun, electron optical column, alignment system, blanker, electron detector and a vacuum chamber which contains a laser controlled stage for providing accurate position of the substrate [25]. In Figure 2.4 the elements in a typical EBL system are shown. A vacuum system provides proper atmosphere inside the column and keeps it safe from the outside environment. The electron gun emits the electrons which passes through numerous additional stages in the electron optical column. Specific beam modification processes such as required current, spot size, and focus are performed in this stage. The electrons are emitted and accelerated by voltage and the beam is aligned in the center by an alignment system inside the column. Magnetic lenses focus the beam and the blanker is used to turn the beam on and off depending on requirement. In this stage, blanker passes the beam to the deflector for scanning. Ultimately, an objective lens focuses the beam which is then propagated onto the substrate.

After the beam is propagated to the substrate it starts to penetrate into the resist, creating a forward and backward scattering. The reason for forward scattering is due to the interaction between electron and electron which produces the broadening of the line width. However forward scattering can be controlled by applying appropriate high accelerating voltage if necessary [26]. Backscattering occurs due to the proximity effect phenomena which is created by the interaction of electrons and atoms presented in the substrate. Because of this effect the scattered electrons starts to propagate into the unplanned part of the resist, thus broadening the line width incompatibly [27]. The fact of getting high resolution and precision which is obtained by small size of focused electron beam from a small size electron source is the reason for its high applicability [28]. Nevertheless, there are other issues that affects the final resolution of the resulting pattern. Among them are proximity effect, beam current, and exposure dose. But resist properties are considered to be the most significant. The size of beam spot can be varied by adjusting the operating voltage where higher operating voltage results smaller spot size. The line width is mostly manipulated by the forward scattered electrons by applying low exposure. Backscattering tends to dominate forward scattering when high exposure dose is provided which increases the proximity effect. As a result, higher beam energy and lower exposure dose are maintained to achieve smaller groove width, [29]. The proximity effect creates distraction in this fabrication process and that is why the researchers are trying to omit this effect and developing different adjusting methods, such as modifications of the pattern data and adjustment of the exposure dose [30].

EBL is recognized for high precision and resolution which provides optimum performance in the field of fabrication process. Automated patterning and privilege of changing the pattern at any point of the process are the reasons of overlooking the limitations of it.

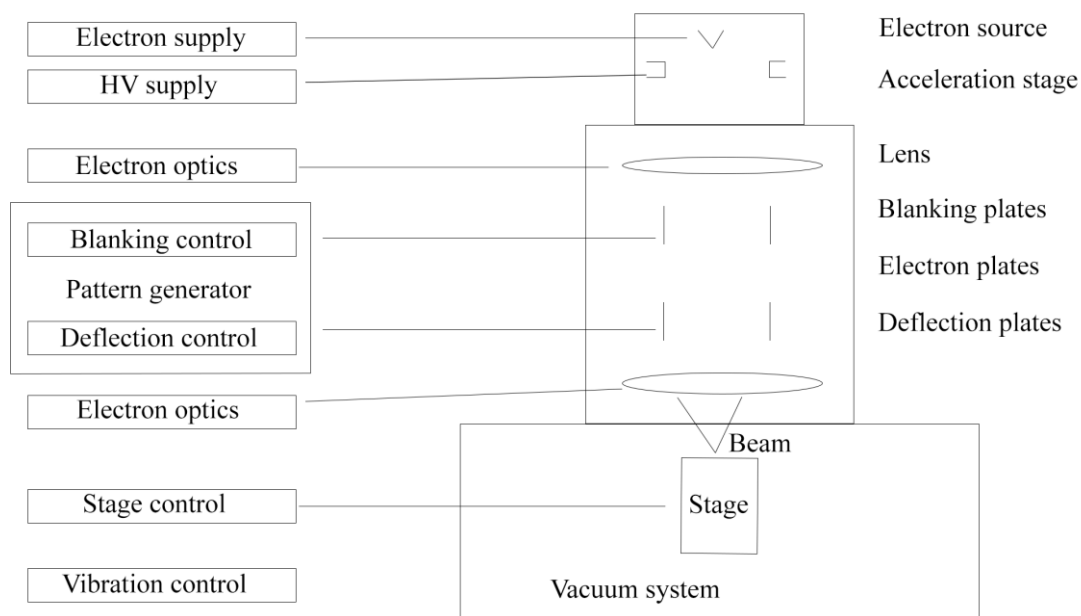


Figure 2.4: An illustration of a conventional EBL system [31].

2.1.3 Resist

Resist is a polymer which is chemically sensitive to radiation (UV) or incident electrons (e-beam). In the first step, a thin layer of this sensitive polymer is deposited on the substrate. Depending on the response of the resist and the radiation it can be of two types—either positive or negative resist. Positive resists are exposed for radiation wherever the material underneath is to be removed. The chemical structure of these resist changes when it is exposed to radiation, making it more soluble in the developer. The exposed resist is removed by the developer which leaves the pattern in the substrate. Thus, while using a positive resist the mask has to have the exact pattern that has to be transferred in the substrate. Negative resists response in opposite way to positive photoresist. When the negative resist is exposed it becomes crosslinked by making the photoresist less soluble to the developer. When it is placed in the developer, the unexposed portion is removed keeping the resist present for the exposed area. Therefore, the mask used for negative resist includes the inverse image of the pattern to be transferred. In Fig. 2.5. the basic difference between positive and negative resist has been presented. During the earliest days of fabrication process, negative resist used to be renowned and still being used for some special features. But the gradual decrease in the pattern size to make the IC compact and to be more controlled, positive resist is used dominantly nowadays in this industry [33].

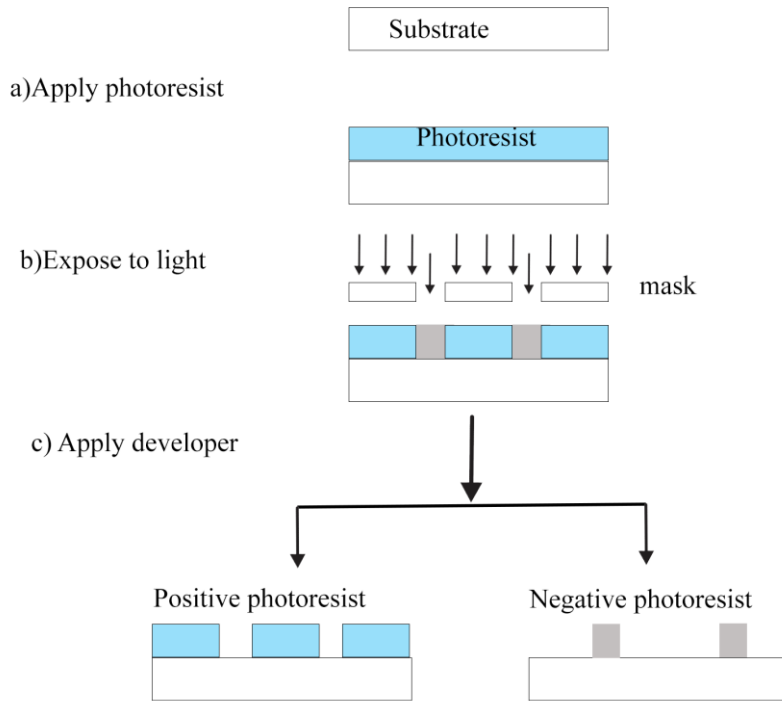


Figure 2.5: Difference between patterns of positive and negative photoresist [32].

2.1.4 Shadow Mask

Patterning metal thin films in a scale of micro or nano dimension under controlled way is always challenging in conventional lithography processes. Interference and back scattering of radiation always affects the resolution of the feature size. Rapid growth of using metal based thin films in IC fabrication created more concern about overcoming these issues. One simple, low cost, reusable technique called shadow mask illuminated these issues. A shadow mask is a thin, micro machined array by which metal or any other material can be deposited directly into the substrate without using any resist in any desired pattern. This masks are also called deposition masks or evaporation masks. It works as a conventional mask in photolithography process during the film exposure process. With shadow mask, it is possible to pattern and deposit metal thin films in microns range[34]. In Fig. 2.6. the schematic illustration of shadow mask is presented. Nowadays, with shadow mask, it is possible to deposit different feature size of thin film in one substrate which is really advantageous for both research and fabrication industry to create mass production of samples at low cost and time.

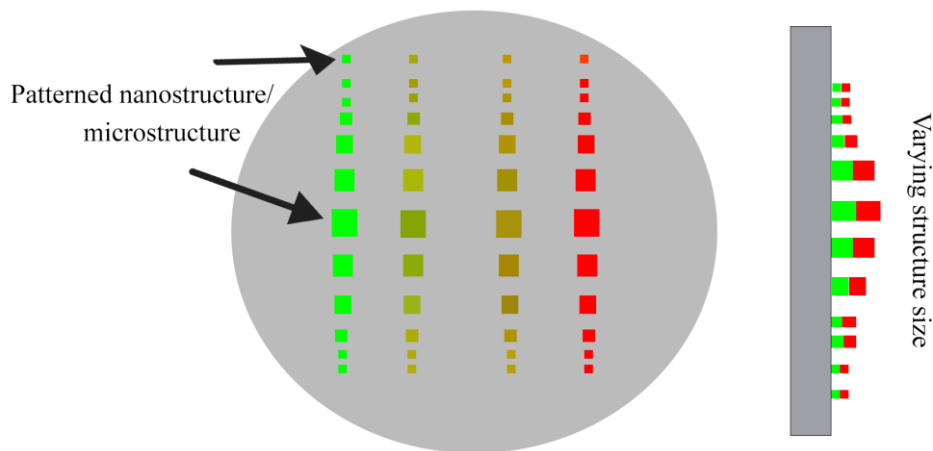


Figure 2.6: Schematic illustration of shadow mask [35].

2.2 Thin Film Deposition

Thin film deposition is one of the crucial and important stages of fabricating micro-nano structured devices. A thin solid film of variety materials is deposited in the substrate by deposition from gas, vapor, liquid or solid for creating conductive layers, insulating or dielectric layer in the substrate with a thickness range of few nanometers to tens of microns [36]. Thin film deposition process is done in two ways-physical by evaporation method or chemical by using gas and liquid based chemical process. The two most popular techniques for mask material deposition are Physical Vapor deposition(PVD) and Chemical Vapor Deposition (CVD). However, there are several deposition techniques available nowadays such as Atomic Layer Deposition (ALD), spray coating, plating, and oxidation. Based on the target of achieving certain optical property and characteristics, different deposition technique is used in fabrication process as they provide different physical structure on the substrate [37,38]. In this experiment PVD was used for making the gold coating and also for coating an insulating layer on the sample substrates.

Physical vapor deposition(PVD) is one of the most common deposition technique to coat layers of atoms or molecules in the substrate, presented in a vacuum chamber where the vapor phase is created. There are two ways of PVD techniques which are sputtering and thermal evaporation system. In thermal evaporation system, a target material is bombarded by a high intense electron beam. The source is placed at the bottom of a vacuum chamber and intense electron beam is propagated through an electromagnetic field of high induction coils which causes the atoms of source material to evaporate and turn into gaseous phase. These atoms in gaseous phase turns into solid thin layer of anode material by

coating everything in the chamber. This technique is used for coating metals and dielectric material in the substrate [39].

Another PVD system is called sputtering where the target is bombarded by ionized gas such as argon. Radio frequency (RF) or direct current (DC) is used to produce the plasma and ions bombardment. Gaseous plasma is created by the ionized gas which accelerates the ions of the plasma to into transmit into the source material. When the ions come across the source material via energy transfer it is discharged as neutral particles (individual atoms, molecules) which travels in a straight line until it comes across any material. The substrate which is coated with the source materials thin layer is created by these neutral particles. Sputtering technique is regularly used for depositing metals, dielectrics, alloys as a thin film in the semiconductor industry. Anti-reflection, low emissivity coating can be also done with the sputtering technique [40]. In Fig. 2.7 the schematic of a typical physical vapor deposition (sputtering) is presented.

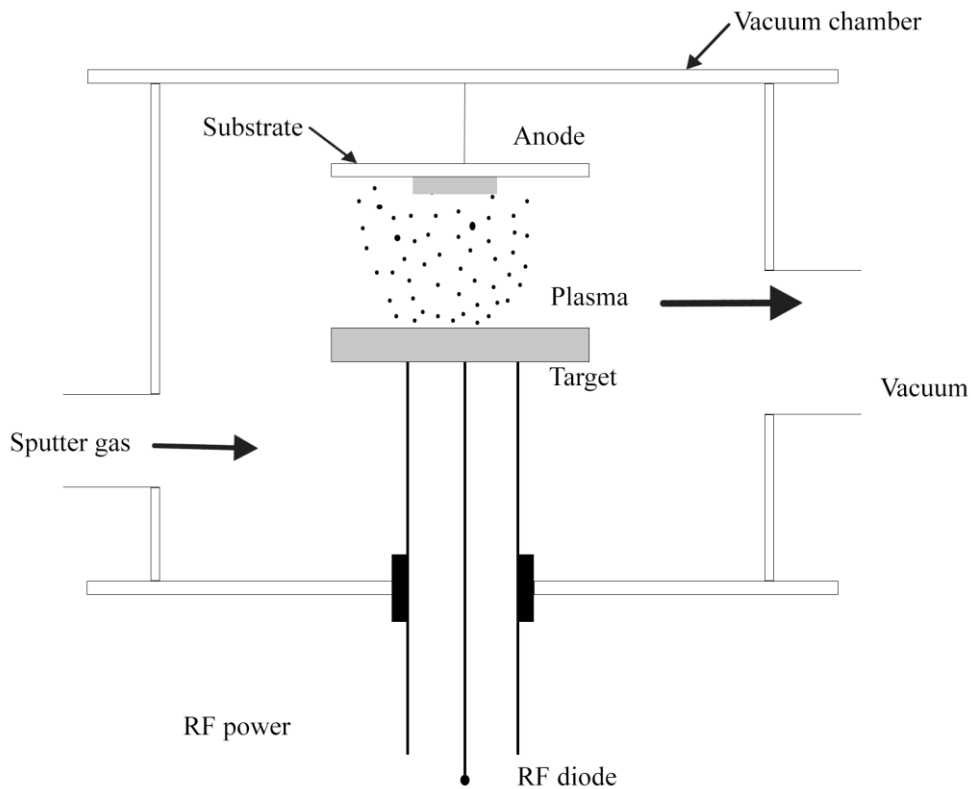


Figure 2.7: The schematic of a typical physical vapor deposition (sputtering) [40].

2.3 Pattern Transfer

Pattern transferring is the process where the resist profile is removed by developer solution. Sometimes the photoresists sidewall profile is necessary for further applications. The three most common type of profiles are- undercut, overcut and vertical profile. For patterning metal, thin films undercut or lift-off profile is used. Overcut profile can be obtained by using positive photoresist. Vertical profile is hard to obtain in all of these

profiles as it has the best side wall among them. For this study, undercut or lift-off profile has been performed as gold thin film was used.

2.3.1 Lift-off

There are several techniques involved in fabrication process for fabricating metallic patterns in the substrate. Patterning metal thin films such as gold, nickel and platinum are considered to be difficult by conventional method of patter transferring. One simple and easy technique of obtaining undercut profile is called lift-off by which the pattern is transferred to the substrate by photoresist. Afterwards metallic thin film is deposited all over the substrate by covering the photoresist. The lift off process is done when the substrate is kept in solvent which removes the film along with the photoresist beneath it and leaves only the film on the substrate where the photoresist is not patterned. This technique causes less defects in the substrate as unwanted materials deposited during the patterning is also lifted off while it was kept in the solvent [41]. In Figure 2.6. the actual lift off process has been shown after the lithography process.

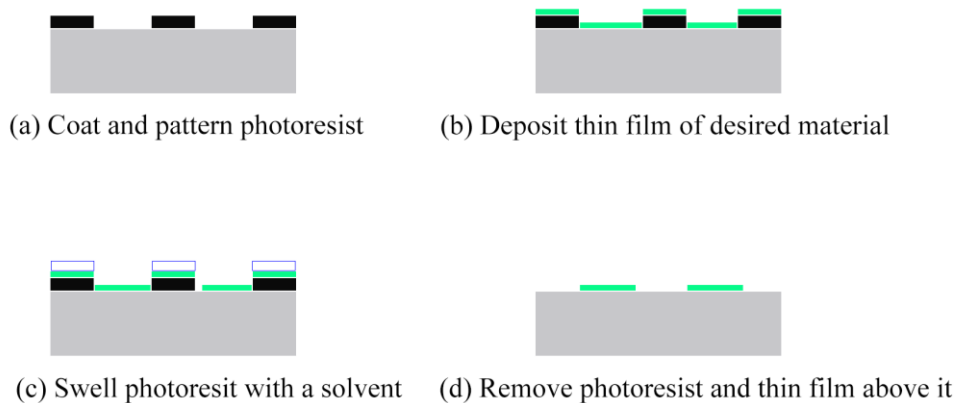


Figure 2.8: An illustration of lifting-off procedure [42].

Although this process takes few steps to implement, few precautions has to be taken during the process. The photoresist has to have opposite polarity than the film. Temperature control is necessary during film deposition as access temperature can burn the photoresist. Also, proper exposure time, proper developer strength and time has to be taken into account for a good lift-off profile.

2.4 Thermal Dewetting

Solid state dewetting of metal thin films is one of the recently developed methods to obtain clear-cut micro-nano structures for applications such as plasmonics, catalysis. Dewetting is the process which occurs in solid-liquid, liquid-liquid interface and it represents the rupturing of thin film on the substrate [43]. The rupturing process involves the surface diffusion of the thin film which influences to change the morphology and forms nanopore or nano sized droplets [44]. This phenomenon in the substrate occurs due to the change of surface energy of the thin film. When the substrate is heated surface energy of the thin film intends to decrease which eventually decreases the interface energy between the substrate and film. So basically, it is a process which occurs due to atomic diffusion [45]. The dewetting process does not only take place over the melting temperature of the thin film, it can occur below the melting temperature. When the dewetting process occurs below the melting temperature than it is called solid state dewetting [46]. Void nucleation is the reason of this process. The creation of grain boundaries and grain boundaries along the interface of metal thin film and substrate influences void nucleation. The creation of grain boundary grooves can be explained by the dissipation of the crystallization effect formed in the interface of the film/air/substrate. This interface is called triple line and for dewetting process the energy for this triple line has to be minimized by satisfying the Smith equation [47]. Thus, continued evaporation of metal thin films leading towards solid state dewetting could be process of etching silicon substrate. Solid state dewetting of gold thin films have been investigated for long time and a widespread view is presented by Müller and Spolenak [48]. The morphological change of gold thin films and the rise of the particles size has been investigated by evaporating the substrate. It is found that the thickness of the deposited gold particles tends to increase and forms into bigger particle packed in the substrate. This phenomenon generally occurs in a line-patterned substrate [49]. This investigation was briefed by Moore and Thornton in 1959 when they performed the research to form the bond between gold and fused silica [50].

Etching Procedure by Gold Nanoparticles

In this chapter, the experimental procedure for etching quartz with the gold nanoparticles will be explained briefly along with the equipment that has been used to develop the process. The brief description of the sample processing and process of patterning will be discussed first. Secondly, deposition of gold and evaporation process to form pores to etch quartz will be described. After all the experimental processes the samples were characterized by the scanning electron microscope. The equipment and tools involved in this experimental procedure are listed in the Appendix A.

3.1 Sample Processing

The samples investigated in this experiment were processed with two techniques. First processed samples were prepared by standard photolithography process. Second process involves the fabrication of a shadowmask where gold thin film was deposited by sputtering on the substrate. In total 14 samples were fabricated by varying different parameters which affects the etching process, such as different thickness of gold nanoparticles and time of evaporation. Also, bulk gradient samples were created by using sputtering techniques to observe the dewetting process. Out of 14 samples 6 samples were prepared from oxidized silicon substrate. Rest of the samples were prepared by using fused silica(SiO_2) substrate to observe the etching characteristics. Except a sample with 40 nm thick gold layer, 20 nm thick layer of gold was deposited in the most of the samples. Temperature from 900 -1070°C was used for the evaporation process for etching. The brief description of the whole fabrication process flow is given in the following sections.

3.1.1 Wafer Cleaning

Silicon substrates are considered to be most common platform for fabrication. They require careful cleaning to remove dust particles and residues from the surface. There are various methods involved in cleaning of silicon wafers. In this experiment, silicon wafer was placed in a beaker with pure acetone in it and kept in an active ultrasonic washing unit nearly about 3 minutes. The wafer was rinsed with isopropanol and then washed with distilled water. Finally, the wafer was dried with nitrogen blower.

3.1.2 Oxide Growth

Along with fused silica substrate oxidized silicon wafers were also used in this experiment. A layer of oxide was created in the substrate as an insulating layer. The process was done by heating the wafer in an oxidized oven for 4 hours in 1050°C and, after this the thickness of the oxide layer was 300 nm.

3.2 Patterning by Photolithography Process

After preparing the wafer it has been taken for patterning. At first, the patterning was done by standard photolithography process. After the photolithography process, gold has been deposited on the wafer and lift off method has been used for transferring the pattern and removing the resist. Photolithography process consists of several steps. The entire procedures followed for this process are discussed with detailed working principals of each instrument below, with an illustration in figure 3.1.

3.2.1 Resist Spinning & Soft bake

After the wafer is cleaned and brought into room temperature, an adhesive layer is deposited on the wafer to improve resist addition. TI PRIME is used as the adhesive layer. Headway spinner PWM101D is used for spin coating the monolayer. At first the substrate was cleaned by blowing nitrogen and placed in the rotating helm of the spinner. The wafer is then spun with a speed of 2000 rpm and 2 ml of TI PRIME was discharged by a pipette in the center of the helm. The substrate was spun for approximately 20 seconds to coat a layer of 3 nm of TI PRIME monolayer on the substrate. After the spin, it was made sure that no residual drops are present in the wafer. The wafer is than placed onto HP ATV, a preheated hot plate and kept for 2 minutes in 120°C temperature for soft baking. This adhesive layer is only coated for photolithography patterning process to be used with lift off technique.

After coating the adhesive layer, the substrate was proceeded for resist coating. The resist, that was used for the lithography process, was S1805 positive resist. Before applying the resist, the spinner was cleaned with acetone for a minute so that there is no TI PRIME left in the spinner. After cleaning the spinner, the substrate was placed in the rotating wheel and 2 ml of photoresist was deposited in the center of the wheel by a pipette. The spin speed was 1500 rpm for a thickness of 700 nm of photoresist on the substrate. The spin time was set to 60 seconds. After the resist addition, the substrate was kept in the pre-heated hot plate for 60 seconds in 110°C to remove remaining solvents and to support adhesion of the resist layer in the substrate. During this time the spinning chamber and rotating wheel were cleaned with acetone.

3.2.2 Exposure

After the resist coating, substrate was taken for patterning by photolithography system. The patterning was carried with the Canon PLA-501FA mask aligner. The resolution of the system is one micron and it has the capability to do both contact and proximity printing. The photomask that has been used for this experiment was a 5-inch fused silica mask. The thickness of chromium in the mask was 100 nm and the mask was patterned by electron beam lithography and Reactive Ion Etching. The surface of the mask has an antireflective oxide coating.

For the photolithography process, the mask aligner Canon PLA-501FA was turned on for 15 mins to warm up the lamp. After warming up the lamp, the current was brought into preferred operation range by adjusting the CURRENT ADJ knob. The valves of 3 utilities nitrogen, air and vacuum were also turned on at this point. For this experiment, hard contact mode was used where vacuum is used to align the mask and substrate together. After choosing the contact mode, the photomask is loaded on the photomask plate. The mask was aligned with guided pins in the plate and then 'load mask' button was pressed to hold the mask in the vacuum ring. After loading the mask, wafer was loaded in the system. An auto hand does the calibration between the mask and substrate. The alignment gap between the mask and substrate was 30 μm . Contact between the mask and substrate can be observed by observing interference fringes in the mask aligner system. After loading the wafer, the exposure process was performed for around 10 seconds. The development process was for about 1 minute. After which, the wafer was taken from the auto hand after the operation and the mask was safely kept in the mask box. The system was turned off after closing the gas valves carefully.

3.2.3 Deposition of Gold

After patterning, the substrate was taken to deposit gold thin film. The gold thin film was deposited by Emitech K675X sputter coater system. This sputter coater system provides thin and even coating by employing magnetron target. The system consists of three target assemblies which provides coating throughout a large diameter with a rotating sample table. It also contains twin gear rotating sample stages which provides advanced elliptical rotation for even deposition. For this process the substrate was carefully attached in a holder and kept in the stage. Gold target plate was placed in the target assembly and the metal ring was carefully screwed to make sure that the target is in the center. Tool factor for gold, 2.5, was chosen. Argon gas valve was turned on to create plasma in the system. The pressure for argon valve tap was set 0.5 bar. Plasma ions, created from argon, strikes the gold target and ejected gold atoms diffuse towards the substrate. Thus, a thin gold film was deposited on the substrate. The terminate value which is the thickness of gold was chosen as 20 nm or 40 nm. After the deposition, the chamber is opened and the substrate was taken out carefully.

3.2.4 Resist Development

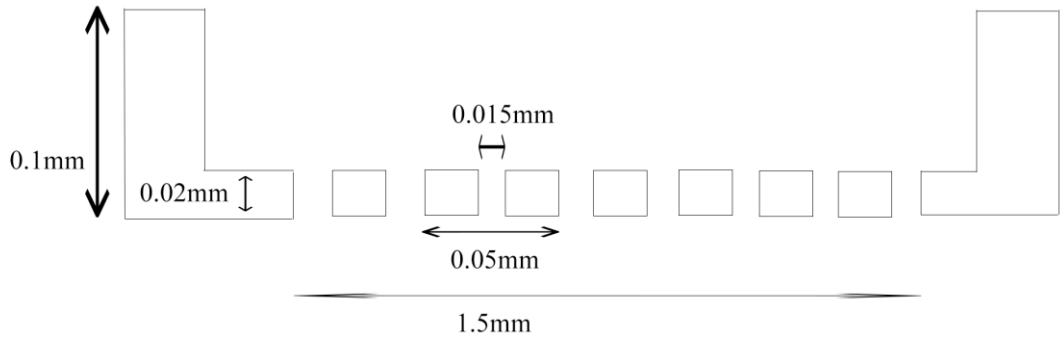
For the resist development process the substrate was deposited in a wet developer. The developer was prepared from sodium hydroxide solution. In a beaker 10 ml sodium hydroxide solution is mixed with 50 ml of distilled water. After preparing the developer the substrate was kept in there for a minute. After that, the substrate was taken out from the solution and dried with the nitrogen blow.

3.2.5 Lift-off

After depositing the gold thin film, lift off method was performed to transfer the pattern on the substrate. The mask plate that was used for patterning had several hole patterns and gold was deposited by that pattern. There were square shape grid and hexagonal grids in the mask. The hole diameter for square shaped grid was 2 μm . In 5 μm diameter hexagonal grid, there were 1 μ and 2 μ holes. To remove the photoresist, lift off method was performed. For lifting off the resist, acetone was used as a solvent. For that acetone was taken in a beaker and substrate was placed in it. The beaker was placed in the ultrasonic unit for a minute to remove the resist. Acetone dissolved the photoresist stencil underneath the layer of gold. The substrate was taken out from the solvent carefully after the pattern of gold was properly visible and lifting off of the photoresist. Substrate was than dried with nitrogen blow and placed in the holder.

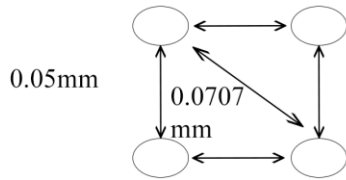
3.3 Patterning by Shadowmask process

Another patterning technique involved in these experiments was the usage of a shadowmask. For the shadowmask process the wafer was cleaned and prepared in the same way as described in the sample processing section. After preparing the wafer the shadowmask is prepared. The shadowmask used in this experiment was 100 μm thick silica film where 20 μm and 15 μm holes were present. The distance between two adjacent holes was 50 μm and the distance of each grid was 1.5 mm. Details of the shadowmask are shown in figure 3.1. At first the mask was cleaved into preferred size with a scissor carefully. The mask was then attached in the center of the substrate by using an adhesive tape. The substrate was then taken for depositing gold. The deposition of gold was done by Emitech K675X sputter coater system. After sputtering the substrate was taken out from the system and the shadowmask was removed carefully. After removing the shadowmask the substrate was put in the holder.

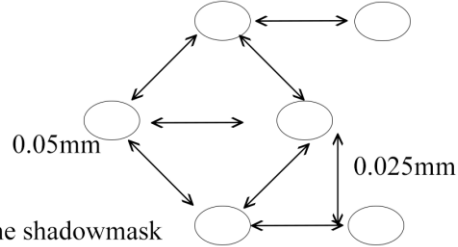


a) Cross section view of the shadowmask

Distances between holes in square pattern



Distances between holes in hexagonal pattern



b) Top view of the shadowmask

Figure 3.1: Illustration of the shadowmask used for the experiment.

3.4 Patterning by bulk gradient process

The third patterning process that was used was bulk gradient process. This process doesn't include any mask to fabricate gold nanoparticles. For this method, the substrate was kept vertically tilted during the sputtering process. As we have used Emitech K675X sputter coater system which uses magnetron sputtering, the ions of the target material always move vertically downwards. Thus, coating the substrate of target material. When the substrate is kept tilted, the thin film is unevenly deposited on the substrate creating a bulk gradient in the substrate. The substrate was kept in the sputter system for 3 minutes to obtain a mask thickness of 20 nm of gold nanoparticles. The detailed illustration of this process can be found in figure 3.3.

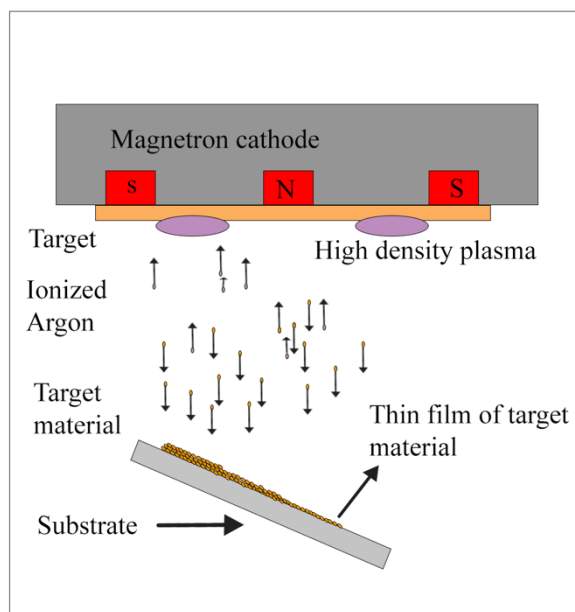


Figure 3.2: Detailed illustration of bulk gradient process.

3.5 Oven treatment

After patterning, the substrates were taken for etching. For this process, high temperature oven was used. Temperature ranged from 900°C-1090°C was kept during the evaporation process. The substrates were kept carefully in the middle of the oven. Necessary personal protection such as protective gloves were used. Digital thermometer was used to measure precisely, the temperature inside the oven. In this research, the evaporation method was carried by two ways. In the first approach the oven was preheated to desired temperature close to 1050°C and substrate was kept there for certain period of time. In the second approach the substrate was kept in the oven starting from the room temperature and slowly heated till 1050°C. After the thermal evaporation, substrates were kept in room temperature to cool down and then placed in the holder.

3.6 Characterization

The samples were characterized with the help of Scanning Electron Microscope(SEM). The sample was cleaved into pieces down through the patterned holes to investigate the

cross-section of the holes. Using the glass cutter pen a sample was scratched on the both side of the substrate. The substrate was then twisted and split into pieces.

3.6.1 Conductive Layer Coating

Some of the sample substrates used in this experiment were not coated with oxide layer. For characterization process it was necessary to coat a conductive layer on the substrate. Copper was used to create a conductive layer over the cross-section of the substrates for SEM imaging. The coating was created using Emitech K675X sputter system with tool factor 3. Argon gas was used to form plasma in the system. The thickness of the coated layer was 7 nm.

3.6.2 Scanning Electron Microscope Imaging

A SEMLEO 1550 Gemini system was used to investigate the cross-section profile of the substrate. At First, the chamber venting was executed from 'Vacuum' tab by choosing Vent in the control software for the system. The sample was then mounted in a sample holder that holds the sample vertically for taking cross-section images. After venting the system, the sample holder was placed in the chamber and the chamber door was closed. By selecting 'Pump' in the 'Vacuum' tab, pump down process was initiated. Once the 'Vacuum Status' was in 'Ready' state, 'EHT' to 'On' was switched from the 'Gun' tab. Through the system control panels display; the sample was adjusted and positioned under the lens by the position knob. After that 'Camera' was switched from ordinary camera mode to the SEM mode. The scanning speed was adjusted to achieve clear images. By using low magnification, the nanopores created on the sample was found. After finding the nanopores the magnification was increased to 50000X. When performing low scanning rate, the stigmation and focus buttons were adjusted simultaneously for clear image. The penetration depth of the nanopores were measured and the image was taken by freezing the live scan. All measurements, such as mask thickness, nanopore height, width, etc. were achieved using the magnification of 50000X. To investigate the sidewall surface roughness, images were taken at higher magnification.

Results and Discussions

In this chapter, analysis and comparison of different effects related to these experiments are presented. Different parameters were taken into account while performing the experiments. The usage of different substrates, patterning processes, evaporation times and rates were considered as the important parameters. These parameters were important for observing the possibilities of surface diffusion process of the fused silica substrate by gold nanoparticles. Penetration depth of gold nanoparticles was investigated according to these parameters. Surface roughness and polymer deposition were also investigated to find the best profile. The etching possibilities of two different mask thicknesses of gold 20 nm and 40 nm were also analyzed and evaluated. Penetration of gold through the surface of the substrate was observed for every samples. However, due to unavailability of Electron Beam Lithography, more precise and high resolution patterning was not possible.

From all the parameters involved in this research, the influence of annealing was considered to be one of the most important fact as Smith equation has to be satisfied for the penetration of gold in the substrate. Also, time controlled continuing evaporation of gold causes the gold nanoparticle to move into the silicon substrate. It was observed that annealing the gold nanoparticles in high temperature close to its melting point influences surface diffusion of the gold nanoparticles in the substrate.

During the initial phase of the experiments, the patterns of gold nanoparticles were not homogenous with photolithography process which was noticed by using the optical microscope. The back reflection of UV during photolithography process was the reason for the pattern no to be homogenous.

Shadowmask process provided better and more homogenous pattern by which the penetration profile was investigated properly. The penetration of gold nanoparticles was not homogeneous for a sample due to improper heat distribution in the substrate. As a result, more precise temperature controlled oven was necessary to carry out the research. It is worth to mention that this research requires further investigation with better patterning procedure and better evaporation technique.

4.1 Result of using different samples

At the beginning, fused silica substrate of 1 inch diameter was used to observe the behavior of the gold nanoparticles deposited in there by shadowmask process. The thickness of the gold nanoparticle was 20 nm. Another sample with 20 nm thickness was prepared by lift off method on oxidized silicon substrate of 100 mm diameter. Formation of gold cap was found in both samples.

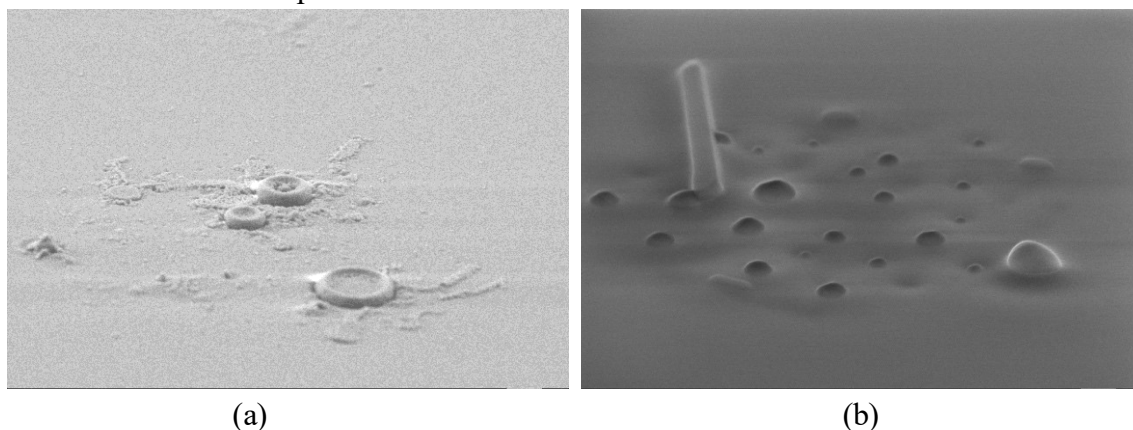


Figure 4.1: (a) Formation of SiO_2 ridge and gold cap of thickness 20 nm on a fused silica substrate which was evaporated for 75 minutes in 1050°C temperature. (b) Formation of SiO_2 crease and gold cap of thickness 20 nm on an oxidized silicon substrate which was etched for 195 minutes in 900°C temperature and 70 minutes in 1073°C temperature.

For the oxidized silicon substrate, it is observed that the diameter of gold cap is different because of improper heat distribution causing less self-diffusion of gold particles. Also, the gold cap tends to penetrate the oxide layer by about 30 nm. The cross-section image of these samples shows the penetration in the case of both samples. The gold nanoparticles tend to penetrate in the silicon substrate. This indicates that with better temperature control it is possible to etch the substrate by gold nanoparticles. Figure 4.2 represents the cross-section of both substrates.

Both of these substrates were prepared by the shadowmask process where 20 nm gold was deposited by sputtering coater system.

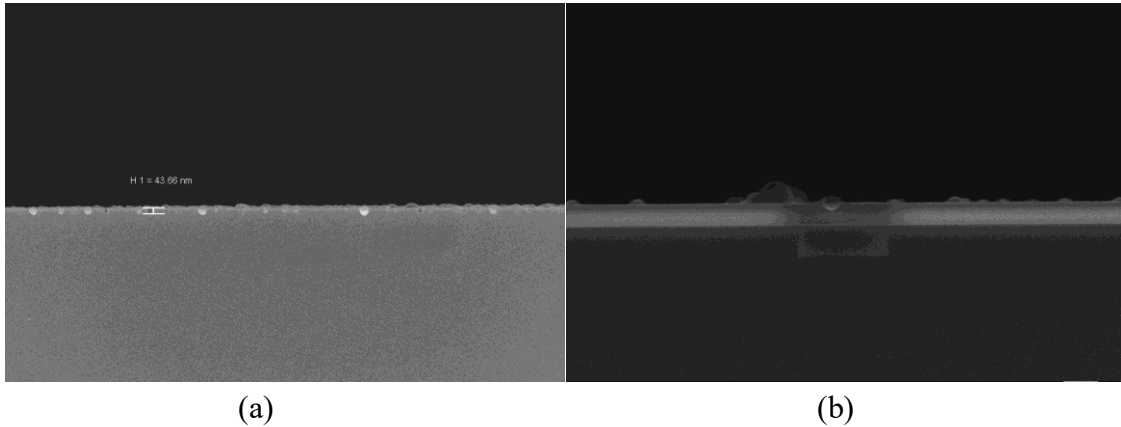


Figure 4.2: (a) Cross-section image of the fused silica substrate shows the penetration of gold nanoparticles on the substrate surface by about 45 nm. (b) Cross-section image of the oxidized silicon substrate which shows the penetration of gold nanoparticles in the oxide layer deposited on top of the substrate.

4.2 Effect of different deposition rate

After observing the penetration process, two samples were created from fused silica substrate with different thickness of gold nanoparticles. The thicknesses of gold nanoparticles were 20 nm and 40 nm which were patterned by shadowmask process. The samples were kept in 1050°C temperature for 75 minutes to observe and compare the penetration of gold nanoparticles and formation of SiO₂ crease. It has been seen that gold nanoparticles tend to penetrate more for higher mask thickness. The reason could be that higher mask thickness influences more surface diffusion of gold nanoparticles which influences tension to the SiO₂ bulge. Morphological change of gold nanoparticles was observed in this process. Results of this observation is presented in figure 4.3.

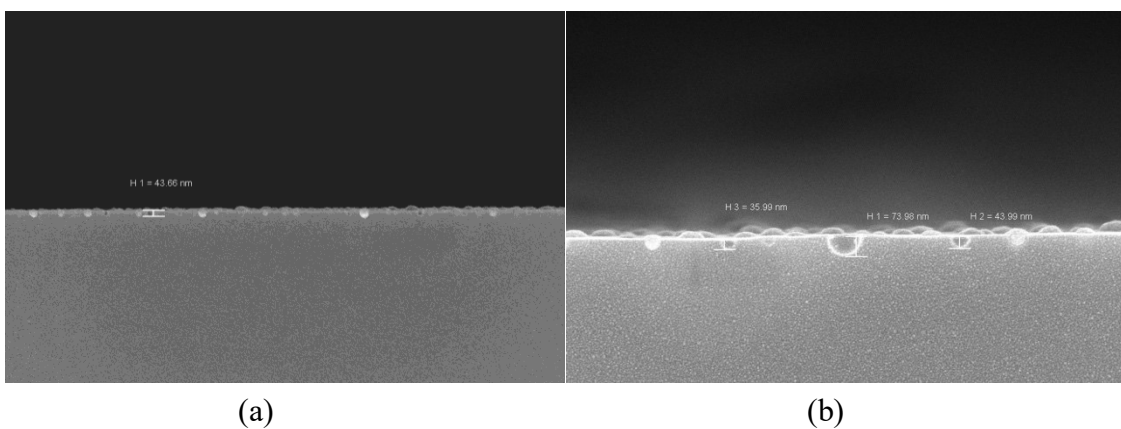


Figure 4.3: (a) Penetration of gold nanoparticles of mask thickness 20 nm by about 45 nm (b) penetration of gold nanoparticles of mask thickness 40 nm by about 75 nm.

4.3 Effect of Annealing

The proposed process has been also observed by the effect of annealing. The experiment was carried out to observe the influence of heating towards gold nanoparticles. For this observation fused silica substrate was used and patterning was carried away by shadow mask process. 20 nm thick layer of gold was deposited on the substrate. At first, the oven was preheated to coarsening temperature of 1050°C. This temperature was chosen to ensure that the morphological change of gold nanoparticles is fast enough. The substrate was placed in the oven from room temperature to high temperature to observe the temperature shock effect of the substrate. For the second method, the oven was kept in the room temperature of 25°C and the substrate was placed in the oven and slowly heated upto 1050°C. The penetration rate was higher for the fast annealing process compared to slow annealing process. Self-diffusion of gold nanoparticles was too slow for the slow annealing process as the substrate surface could affect the change of surface diffusion rate. The annealing effects are shown in figure 4.4.

From this observation, it can be said that the annealing process has an effect on the surface diffusion of gold nanoparticles in the silica substrate. Initially, for fast annealing process the pore forms into bigger size by changing their morphology. During the heat treatment of slow annealing, pores were quite stable by changing their morphology just a little. So, it can be said that, the surface diffusion in gold nanopores advances faster in fast annealing process than in the case of slow annealing.

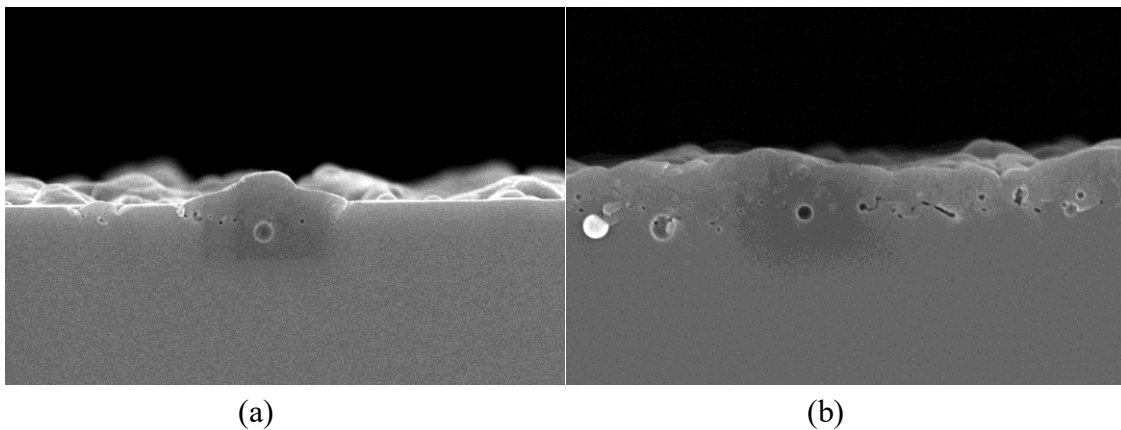


Figure 4.4: (a) Effect of slow annealing process, where the substrate was heated slowly from room temperature to 1050°C in 195 minutes. Morphological change is not observed in this process but ridging of silica substrate is observed with nano pore formation towards substrate. (b) Fast annealing process where the substrate was kept in a preheated temperature of 1050°C for 260 minutes. Morphological change of gold nanoparticles was observed during this procedure as the diameter of gold nanoparticles tend to be increased.

4.4 Result of lift-off method

Another method that is used to observe the behavior of gold nanoparticles surface diffusion towards silica substrate was patterning the substrate by lift-off method. For observing the behavior oxidized silicon substrate was used. The reason for choosing oxidized silicon substrate was to avoid the back reflection of the optical lithography. Standard photolithography process was used for patterning and by sputtering. Mask thickness of the gold was 20 nm. Profiles found in lift-off method are illustrated in figure 4.5.

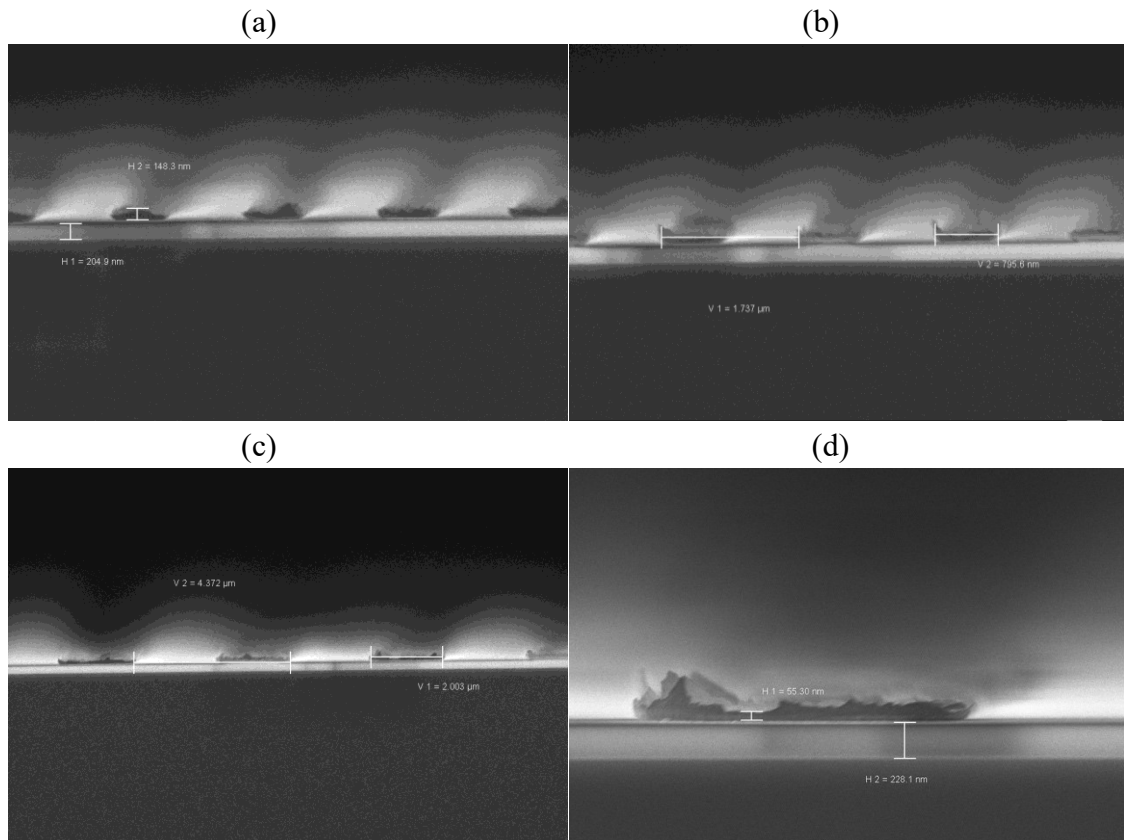


Figure 4.5: (a) Profile found in the 1 μm diameter sized holes part of the substrate. Thickness of gold cap was found about 150 nm and oxide layer thickness was found to be around 210 nm. (b) About 2 μm spacing was found between two adjacent holes with a hole size of around 800 nm (c) Profile found in the 2 μm diameter sized holes part of the substrate was with 4.4 μm spacing between two adjacent holes size of 2 μm . (d) The thickness of gold achieved in this part was around 55 nm. It is also necessary to mention that due to lift-off process uneven distribution of gold was found in the sample.

After lift-off process, the substrate was kept in the oven for thermal treatment by varying the temperature. First samples were heated in 1050°C temperature by slow annealing. Second samples were heated in 900°C with slow annealing process and again heated by

fast annealing process in 1073°C temperature. The results are shown in figure 4.6 with detailed information.

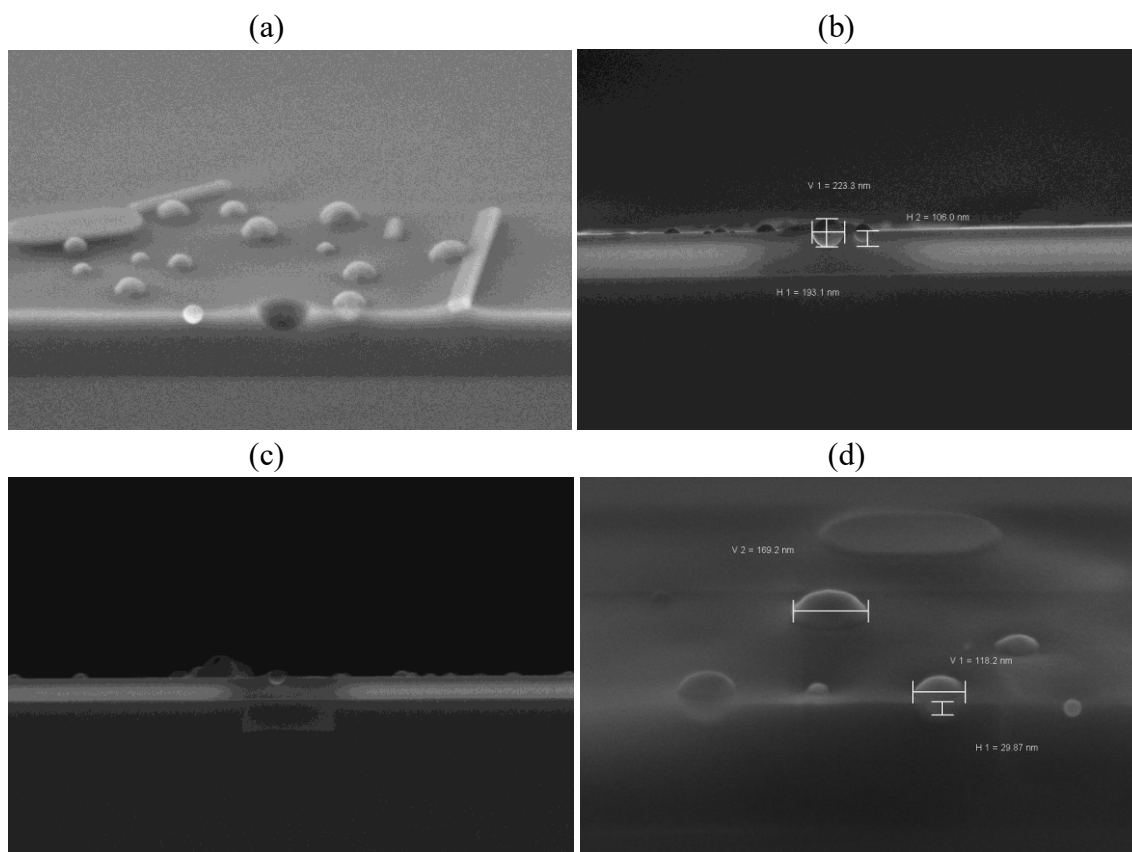


Figure 4.6: (a) Profiles found in oxidized silicon substrate where 20 nm gold was deposited by lift off method. Tilted image of the substrate illustrates diffusion of gold particles on the silicon substrate for thermal evaporation in 1050°C for 145 minutes. (b) Cross-section image shows the size of the gold nanopores and the penetration depth after evaporation. Gold nanoparticles morphological change can be observed. (c) Cross section image of the substrate which was heated by slow and fast annealing process in 900°C & 1073°C temperature, respectively. (d) Tilted image shows the diffusion & penetration depth of the gold nanoparticles.

Gold nanoparticles tends to have more self-diffusion in the oxidized silicon substrate. Patterned substrates can lead to larger and smaller particle size of the gold nanoparticles although more precise patterning is necessary to avoid uneven distribution of gold in the substrate which effects the self-diffusion of the gold particles in the penetration process.

4.5 Result of bulk gradient process

After the observation of the effect of thickness of gold nanoparticles resulting more penetration depth, substrates were patterned by bulk gradient process where the gold nanoparticles deposition rate is uneven in the whole substrate. For this process both fused silica and oxidized silicon substrates were used. Effect of annealing was also considered in this process. Fast annealing process was used for thermal evaporation. The fused silica substrate was kept in 1070°C temperature for 190 minutes. Results of the fused silica samples are shown in figure 4.7.

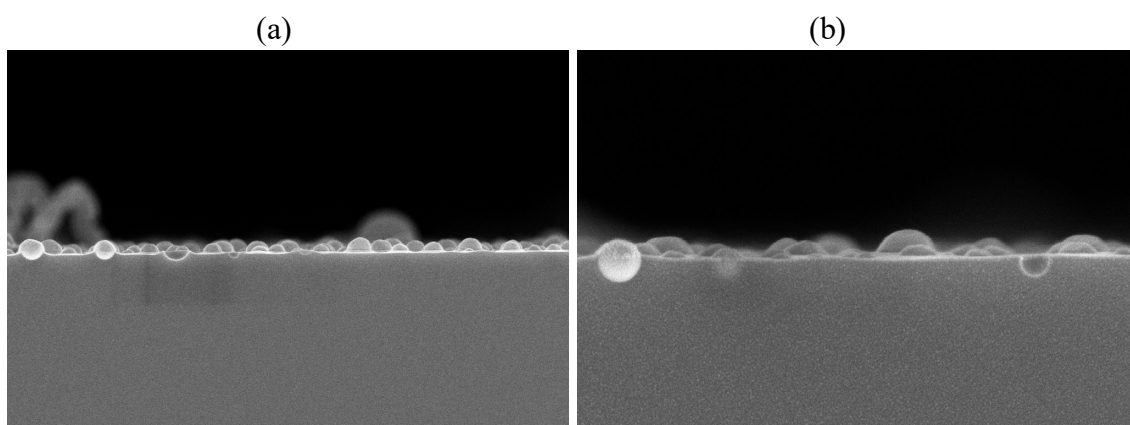


Figure 4.7: (a) Numerous gold caps can be found in the cross-section image of the substrate patterned by bulk gradient process. (b) Formation of SiO₂ crease over the substrate where a few of the nanoparticles tend to penetrate silica substrate.

In the second stage of this process oxidized silicon substrate was used to see the nature of gold nanoparticles. It is seen that gold nanoparticles tend to rapture the oxide layer on the part of the substrate where thick layer of gold nanoparticles is deposited. Gold structures change their morphological structure and creates strain in the silica. The findings conclude that unpatterned substrates with thick layer of gold films can lead to a massive surface diffusion in the silica substrate. It can be also concluded, that gold atoms with the presence of oxidized layer created gold oxide which has more capability to diffuse in the silica lattice. Results of this findings are shown in figure 4.8.

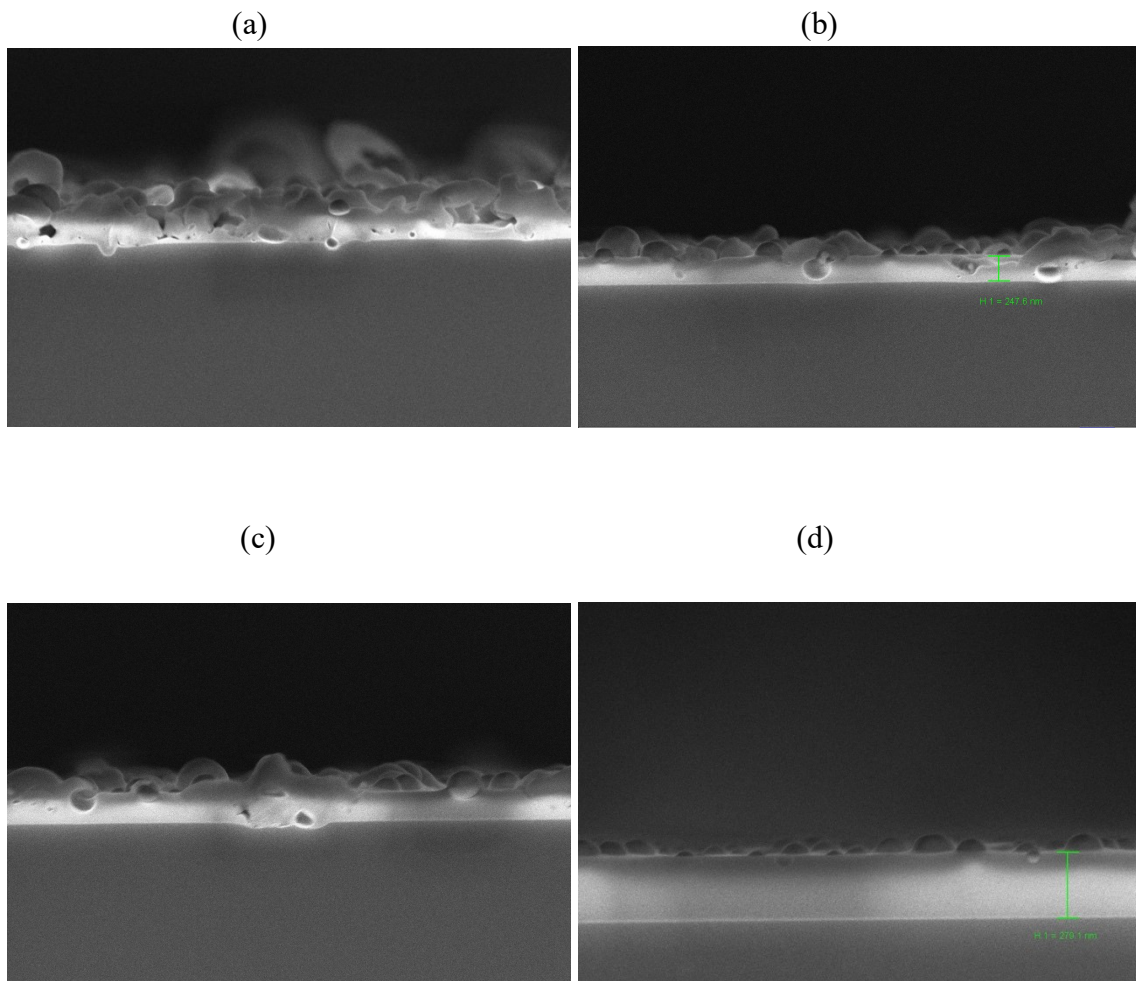


Figure 4.8: (a) thick layer of deposited gold nanoparticles rupturing the silica substrate which was heated for 190 minutes in 1070°C fast annealing process. (b) Change of the thickness of the oxide layer can be seen for the gold nanoparticles diffusion in the substrate. (c) Huge gold caps tends to fracture the interconnection between oxide layer and the substrate by creating SiO₂ bulge. (d) Change in the oxide layer thickness due to surface diffusion of gold nanoparticles.

CHAPTER 5

Conclusions

The etching possibility of quartz by using gold nanoparticles is studied in this work. Penetration of gold nanoparticles in the oxidized silicon and fused silica substrates were observed during the experimental procedure of this work. Depth of penetration by gold particles is examined by using different patterning techniques. The characteristics of gold particles deposited in the substrate is inspected by heating them close to its melting temperature. Analysis of the growth of gold particles caused by self-diffusion is also monitored. Factors affecting the self-diffusion of gold particles such as – thickness of deposited gold, annealing temperature and time are examined in this study. Different patterning techniques provided various penetration depth in the silicon substrate. It can be concluded that gold thin film behavior can possibly be used to etch fused silica substrate with precise patterning and better temperature control.

From the detailed result of this study, it is found that gold nanoparticles create small bulge which after continuing heating forms into nanopore. Self-diffusion of gold nanoparticles causes the nanoparticles to move into the substrate perpendicularly. From the result, evidence of gold-oxygen interaction in the substrate is found for high temperature. Oxide layer deposited in the substrate influences gold nanoparticles to change their morphological structure in a noticeable way. Thus, more depth of penetration is observed in the oxidized substrate than fused silica substrate. In this research, maximum penetration of gold is found close to 200 nm with lift off method.

It is also observed that the thickness of oxide layers also get affected by high temperature as the thickness tends to increase. So, it can be said that gold atoms can penetrate silica lattice better when oxidization is present in the diffusion process. This diffusion process can also be used for pure fused silica substrate by depositing a gold layer on top of it if oxidization oven is used for annealing process. Unfortunately, due to the unavailability of the oven this experiment was not performed in this study.

Etching possibility through shadowmask process and bulk gradient process also provided positive evidence. Penetrated gold nanoparticles after annealing were not homogenous although the gold nanoparticles were homogenous during patterning. For better possibility of etching it can be said that the distance between two adjacent grids can be reduced so that more gold nanoparticles can be deposited in the substrate. As seen from the bulk gradient process bulk number of gold nanoparticles tends to rupture the substrate.

From this study three possible observations are evaluated. Firstly, lateral diffusion of gold nanoparticles along the silicon substrate can possibly be used to etch the substrate with

prolonged and controlled heating. Although it has to be taken into account that prolonged heating close to the melting temperature of gold can devitrify the silicon substrate.

Secondly, the increase of particle size and particle spacing does not only occur on the patterned surface. The increase of particle size in the bulk gradient process clearly proves that surface diffusion of gold nanoparticles can be also achieved without patterning the substrate. Which indicates that the surface energy needed to form two new surface by rupturing the substrate depends on the thermal equilibrium.

Thirdly, type of annealing and thickness of gold nanoparticles has influence on morphological change of gold nanoparticles. It is observed that fast annealing process with higher thickness of gold nanoparticles tends to penetrate the silica substrate more compared to slow annealing process. It can be said that with better temperature control and by satisfying the thermal equilibrium with precise contact angle between the gold and silica substrate it is possible to develop an etching characteristic. Thus, more profound studies can lead into a success on this research.

BIBLIORAPHY

- [1] R. Powell, *Dry Etching for Microelectronics*, Vol. 2, (Elsevier B.V., 1984).
- [2] P.O. Ulanmo, "Oxygen plasma stripping of photoresist from bipolar integrated circuit wafers - process development," *ETD Collection for AUC Robert W. Woodruff Library*. 690. (1981).
- [3] S. Irving, K. Lemons, and G. Bobos, "Gas plasma vapor etching process," (US Patent 3,615,956, 1971).
- [4] N. Hosokawa, R. Matsuzaki, and T. Asamaki, "RF Sputter-Etching by Fluoro-Chloro-Hydrocarbon Gases," *Japanese Journal of Applied Physics*, Vol. 13, pp 435-438, (1974).
- [5] M. J. Kushner, "A kinetic study of the plasma-etching process. I. A model for the etching of Si and SiO₂ in CnFm/H₂ and CnFm/O₂ plasmas," *Japanese Journal of Applied Physics*, Vol. 53, pp 2923-2926, (1982).
- [6] M. Kohler, *Etching in Microsystem Technology*, (Wiley-VCH, 2006).
- [7] J. Wang, H. Niino, and A. Yabe, "One-step microfabrication of fused silica by laser ablation of an organic solution," *Applied Physics A*, Vol. 68, pp 111-113, (1999).
- [8] D. A. Zeze, R.D. Forrest, J.D. Carey, D.C. Cox, I.D. Robertson, B.L. Weiss, and S. R. P. Silva, "Reactive ion etching of quartz and Pyrex for microelectronic applications," *Journal of applied physics*, Vol. 92, pp 3624-3629, (2002).
- [9] M. Sekine, *Dielectric film etching in semiconductor device manufacturing: Development of SiO₂ etching and the next generation plasma reactor*, (Science Direct, Vol. 192, pp 270-298, 2002).
- [10] V.M. Donnelly, A. Kornblit, "Plasma etching: Yesterday, today, and tomorrow", *Journal of Vacuum Science & Technology A*, Vol. 31, 05082, (2013).
- [11] I.R. Christie, B.P. Cameron, *Gold electrodeposition within the electronics industry*, (Gold Bull, Vol. 27, pp 12-20, 1994)

- [12] D. Huang; F. Luao; S. Molesa; D. Redinger; V. Subramanian, “Properties and applications of Gold Nanoparticles”, *Journal of the Electrochemical Society*, Vol. **50**, pp 412-417, (2003).
- [13] A. Sasidharan, N.A. Monteiro-Riviere, “Biomedical applications of gold nano-materials: opportunities and challenges”, *Wiley interdisciplinary reviews. Nanomedicine and nanobiotechnology*, Vol. **7**, pp 779-796, (2015).
- [14] M. E. Ali; U. Hashim; S. Mustafa; Y. B. Che Man; Kh. N. Islam, “Gold Nanoparticle Sensor for the Visual Detection of Pork Adulteration in Meatball Formulation”, *Journal of Nanomaterials*, Vol. **2012**, 103607, pp 2-5, (2012).
- [15] R.C. Jaeger, “*Introduction to Microelectronic Fabrication*”, Ed. 2, (Upper Saddle River: Prentice Hall. ISBN 0-201-44494-1, Vol. **5**, pp 17-35, 2002).
- [16] J. Chopra, “Analysis of lithography based approaches in development of semiconductors”, *International Journal of Computer Science & Information Technology*, Vol. **6**, pp 61-72, (2014).
- [17] R. Zaouk, B.Y. Park, M.J. Madou, *Introduction to Microfabrication Techniques*, (Springer 10.1385/1-59259-997-4:3, pp 5-15, 2006).
- [18] A. Hierlemann, O. Brand, C. Hagleitner, H. Baltes, “Microfabrication Techniques for Chemical/Biosensors”, *Proceedings of the IEEE*, Vol. **91**, pp 839-863, (2003).
- [19] C.A. Mack, “*Fundamental Principles of Optical Lithography: The Science of Microfabrication*”, (Wiley-10.1002/9780470723876, pp 1-28, 2007).
- [20] H. Miyajima, M. Mehregany, “High-Aspect-Ratio Photolithography for MEMS Applications”, *Journal of microelectromechanical systems*, Vol. **4**, pp 162-169, (1995).
- [21] C.A. Mack, “*Enhanced Lumped Parameter Model for Photolithography*”, (SPIE Vol. **2197**, pp 501-510, 1994).
- [22] M. Rothschild, “Projection optical lithography”, *Materials today*, Vol. **8**, pp 18-24, (2005).
- [23] ASML instruments, www-page, https://www.asml.com/products/systems/twinscan-nxe/twinscan-nxe3400b/en/s46772?dfp_product_id=10850.
- [24] M.G.E Hak, “*The MEMS Handbook*”, (CRC Press, Boca Raton, FL, pp 401-526, 2005).

- [25] P. Coane, “*Introduction to Electron Beam Lithography*”, (Institute for Micromanufacturing, pp 1-15, 1997).
- [26] M.A. McCord and M. J. Rooks, “*Handbook of Microlithography, Micromachining, and Microfabrication*”, (SPIE–The International Society for Optical Engineering, Vol. **1**, pp 139-197, 1997).
- [27] T.H.P. Chang, “Proximity effect in electron–beam lithography,” *Journal of Vacuum Science and Technology*, Vol. **12**, pp 1271–1275 (1975).
- [28] Z. Cui, “*Nanofabrication: Principles, Capabilities and Limits*”. (Springer US, pp 91-148, 2008).
- [29] G.R. Brewer, “*Electron-Beam Technology in Microelectronic Fabrication*”, (Academic Press, New York, 1st ed., pp 79-93, 1980).
- [30] G. Owen, “Proximity effect correction in electron-beam lithography,” *Optical Engineering*, Vol. **32**, pp 2446–2451 (1993).
- [31] C.S. Wu, Y. Makiuchi, and C. Chen, “*High–energy Electron Beam Lithography for Nanoscale Fabrication*”, (Creative Commons, pp 249-274, 2010).
- [32] T. Betancourt, L.B. Peppas, “Micro- and nanofabrication methods in nanotechnological medical and pharmaceutical devices”, *International Journal of Nanomedicine*, Vol. **2006**, pp 483-495, (2006).
- [33] M.J. Madou, “*Fundamentals of Microfabrication: The Science of Miniaturization*”, 2nd ed., (CRC Press, Boca Raton, FL., pp 351-370, 2002).
- [34] M. Apanius, P.B. Kaul, A.R. Abramsona, “Silicon shadow mask fabrication for patterned metal deposition with microscale dimensions using a novel corner compensation scheme”, *ScienceDirect, Sensors and Actuators A* **140**, pp 225-229, (2007).
- [35] A. Ludwig, J. Cao, J. Brugger, I. Takeuchi, “MEMS tools for combinatorial materials processing and high-throughput characterization”, *Measurement Science and Technology*, Vol. **16(1)**, pp 111-118, (2005).
- [36] R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, G. Dewey, “30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays”, *International Electron Devices Meeting*, (2000).

- [37] S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, J. Brandenburg, W. Chen, B. Crew, M. Hussein, P. Jacob, C. Kenyon, C. Lo, B. McIntyre, M.A. Zhengchu, P. Moon, P. Nguyen, L. Rumaner, R. Schweinfurth, S. Sivakumar, M. Stettler, M. Bohr, “A 130 nm Generation Logic Technology Featuring 70 nm Transistor, Dual Vt Transistor and 6 layers of Cu Interconnect”, *IEDM Proceedings*, pp 567-570, (2000).
- [38] K. Seshan, T. J. Maloney, K. J. Wu, “Quality & Reliability of Intel’ s 0.25 μm Process”, *Intel Technology Journal*, (1998).
- [39] B. Ziaie, A. Baldi, and M. Atashbar, “*Introduction to Micro-/Nanofabrication*,” (Springer Berlin Heidelberg, pp 147-184, 2010).
- [40] D. M. Mattox and K. Firm, “*Handbook of physical vapor deposition (PVD) processing: film formation, adhesion, surface preparation and contamination control*”, (Westwood, N.J.: Noyes Publications, pp 236-244, 1998).
- [41] S.C. Chang, J.M. Kempisty, “*Lift-off Methods for MEMS Devices*”, Vol **729**, (Mat. Res. Soc. Symp. Proc., pp 1225-1257, (2002).
- [42] M. Hatzakis, B.J. Canavello, J.M Shaw, “Single-step optical lift-off process” *IBM-Journal-of-Research-and-Development*, Vol. **24**, pp 452-460, (1980).
- [43] A. Dmitriev, “*Nanoplasmonic Sensors*”, (Springer New York, pp105-127, 2012).
- [44] A.B. Tesler, B.M. Maoz, Y. Feldman, A. Vaskevich, I. Rubinstein, “Solid-State Thermal Dewetting of Just-Percolated Gold Films Evaporated on Glass: Development of the Morphology and Optical Properties”, *The journal of physical chemistry*. Vol. **117(21)**, pp 11337-11346, (2013).
- [45] A. Herz, M. Fri.k, D. Rossberg, M. Hentschel, F. Theska, D. Wang, D. Holec, M. Šob, O. Schneeweiss, and P. Schaaf, “Imaging the absolute configuration of a chiral epoxide in the gas phase”, *Applied Physics Letters*, Vol **107**, pp 1084-1086, (2015).
- [46] A. Herz, a A. Franz, F. Theska, M. Hentschel, Th. Kups, D. Wang, a and P. Schaaf, “Solid-state dewetting of single- and bilayer Au-W thin films: Unraveling the role of individual layer thickness, stacking sequence and oxidation on morphology evolution”, *AIP Advances*, Vol. **6**, (2016).
- [47] I.J.D Vreede, A.V.D berg and J.C.T Eijkel, “Evaporation-driven nanomachining to fabricate nanopores in sio₂”, *MicroTAS*, pp 1844-1846, (2014).

- [48] C. M. Muller and R. Spolenak, "Spectroscopic investigations of ammonia gas sensing mechanism in polypyrrole nanotubes/nanorods", *Journal of Applied Physics*, Vol. **113**, (2013).
- [49] D. Wang, P. Schaaf, "Thermal dewetting of thin Au films deposited onto line-patterned substrates", *Journal of Materials Science*, Vol. **47**, pp 1605-1608, (2011).
- [50] D. G. Moore and H. R. Thornton, "Effect of Oxygen on the Bonding of Gold to Fused Silica", *Journal of Research of the National Bureau of Standards*, Vol. **62**, pp 127-138, (1959).

Appendix A

Used Equipment's

- Canon PLA-501FA mask aligner.
- Emitech K675X.
- Headway spinner PWM101D.
- OPTIspin SST20.
- Automatic dicing saw DAD3240.
- Plasmalab 80 plus.
- Leo 1550 Gemini.
- Ultrasonic cleaning machine.
- Hot plate.
- Glass cutter pen.
- Nitrogen gun.
- Vacuum oil.
- Tweezers, scalpel, pipette, beakers and scotch tape.
- Heraeus MR170 oven.